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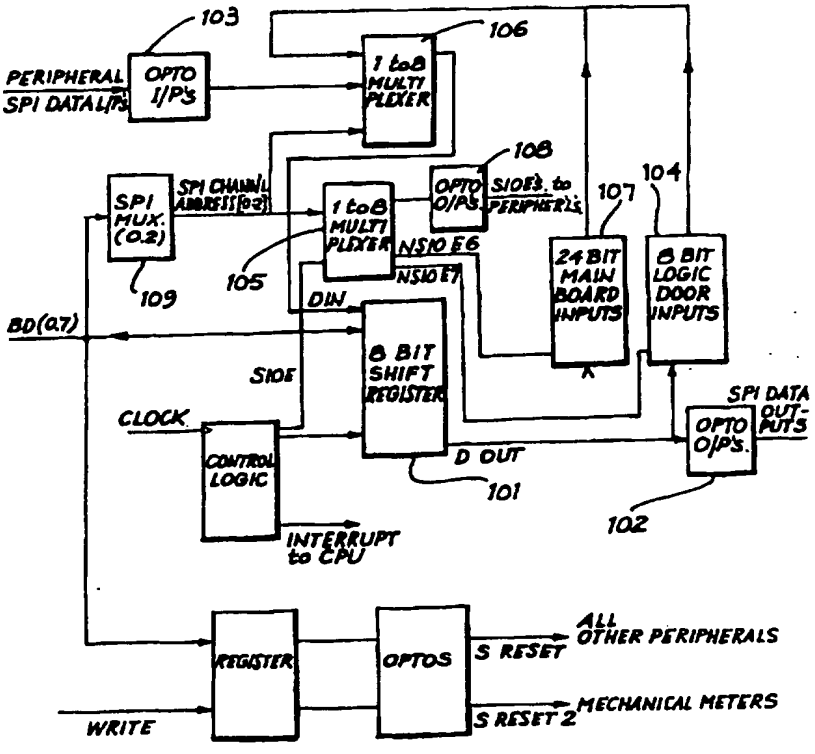
(57) Abstract

The Serial Peripheral Interface (SPI) is designed to drive multiple SPI peripherals via a simple serial connection. The number of devices controlled is easily expanded without modifying the looming or main board interface. Peripheral outputs are provided by a power driver chip which drives fully protected output channels from the SPI interface. Each channel is short circuit and overvoltage protected, with diagnostic fault readback of short and open circuits. Peripheral inputs use CMOS logic parallel load shift registers, which are easily interfaced to the SPI.



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SERIAL PERIPHERAL INTERFACE

Introduction

The present invention relates generally to slot machines and in particular the invention provides an improved signal distribution method within a slot machine cabinet.

Typically, in equipment such as slot machines, signals are distributed from a central processing unit via parallel interfaces located in close proximity to the processor, which provide buffered drivers to drive signals which are distributed to points throughout the cabinet via large wiring loom. Such arrangements have the disadvantage that wiring is complex and expensive and that wired looms are susceptible to electrical noise, making it necessary to provide noise protection.

Summary of the Invention

According to a first aspect, the present invention provides a peripheral interface system for a digital processor, the interface comprising parallel input/output (I/O) means arranged to interface with a parallel input/output bus of a digital processing unit, parallel to serial conversion means arranged to convert a data word from the parallel I/O bus to a serial data string on a serial output data line of a serial bus, serial to parallel conversion means arranged to convert a serial data string on a serial input data line of the serial bus to a data word on the parallel I/O bus, clock means arranged to provide timing signals for the interface and control means arranged to control the transfer of data between the parallel I/O bus and the peripheral serial bus, the control means also providing a bus clock. a data enable signal, and a reset signal on the serial bus in addition to the input and output serial data lines.

Preferably the interface provides a plurality of serial buses, each connected in parallel to the serial to parallel and parallel to serial conversion means, the clock means and the control means, there being a separate data enable signal for each channel. In the preferred embodiment 7 serial channels are provided for each parallel interface.

According to a second aspect, the present invention provides a slot machine comprising game playing means and control means wherein the game playing means includes at least one peripheral device and communication between the control means and the at least one peripheral device is via a serial interface system as hereinbefore described.

Preferably a distribution board is provided to interconnect with the serial bus to demultiplex the serial bus output signals and to drive output devices and to receive input signals from input devices and to multiplex these into serial bus signals.

Brief Description of the Drawings

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 schematically illustrates an embodiment of a serial interface system according to the present invention;

Figure 2 is a listing of a source file for a Gate Array Logic (GAL) device used in the control circuit of the serial interface system of Figure 1;

Figure 3 diagrammatically illustrates a timing diagram for the serial interface of Figure 1;

Figures 4 and 5 schematically illustrate two possible configurations for driving mechanical meters from the serial interface of Figure 1; and

Figure 6 schematically illustrates the overall configuration of the serial interfaces provided in the machine of the preferred embodiment.

Detailed Description of the Embodiment

The preferred embodiment of the invention will be described with reference to a gaming machine.

The primary functions of the gaming machine control system are built into an Application Specific Integrated Circuit (ASIC) which provides:

- A central processor
- Dynamic RAM Controller
- Video controller
- Sound generator
- System glue logic
- Interrupt controller
- Clock dividers

The ASIC processor includes several interrupt inputs. From a formal point of view all these inputs along with any signal used to acknowledge the interrupts to the peripherals can be grouped as a bus.

Within this description, the term "Direct Output" refers to those outputs that are directly under processor control either through a parallel port or through an SPI bus. They are not part of a specific bus nor do they follow a protocol like the NRZ protocol of the asynchronous serial interfaces.

The system has two types of Direct Outputs:

1. Slow Direct Outputs
2. Fast Direct Outputs

The Slow Direct Outputs are outputs that control relatively slow devices such as lamps and solenoids. The Slow Direct Outputs can be updated 60 times a second.

The Fast Direct Outputs require immediate processor action. They are normally connected to a parallel output port.

The system has three types of inputs:

1. Slow Inputs
2. Fast Inputs
3. Interrupting Inputs.

The Slow Inputs are inputs that are scanned at relatively low speed. That speed is dependent on the power of the processor and the electronic hardware through which the signal can travel. As they are slow they can be heavily filtered and optically coupled to get excellent noise immunity. The Slow Inputs are scanned 60 times a second.

Fast Inputs are those that are scanned periodically. They are associated with devices that are relatively fast but either they should be periodically read for a particular reason or they can remain unattended for a relatively long time without problem. Most of the handshake lines are in this category and they are normally associated with serial channels.

The Serial Peripheral Interface (SPI) is designed to drive multiple SPI peripherals via a simple serial connection. The number of devices controlled is easily expanded without modifying the looming or main board interface. An overall block diagram of the SPI interface is illustrated in Figure 6 and a block diagram of the conversion and control arrangement is illustrated in Figure 1.

Peripheral outputs are provided by a power driver chip (refer to Figures 4 and 5) which drives fully protected output channels from the SPI interface. Each channel is short circuit and overvoltage protected, with diagnostic fault readback of short and open circuits. These control the lamps and mechanical meters.

Peripheral inputs use CMOS logic parallel load shift registers, which are easily interfaced to the SPI. A range of chips is suitable for this purpose. The door buttons are read using this interface.

The SPI interface uses 4 output signals and 1 input signal. These are:

Signal Name	Function
NSIOE	Serial I/O enable output
DOUT	Data output
CLK	Clock output
NRESET	Reset output
DIN	Data input

The serial interface system is designed around an SPI controller, whose outputs and inputs are multiplexed onto one of seven channels via an SPI Channel address.

At the start of an SPI transfer the NSIOE signal is asserted (low). The first data bit is transmitted, then the clock raised to allow the SPI devices to clock in the data. The data input, DIN, is read back into the shift register. Each subsequent bit is shifted out and clocked, until all 8 bits have shifted out, whereupon an interrupt will be generated to the CPU. The CPU will then start the transfer of the next byte, or negate NSIOE to end the cycle.

The main door interface uses 2 SPI channels to scan the button switches and control the button lamps. The switches need to be read at a relatively high rate to give good button response. The lamps are updated at a slower rate, especially when they do not change. Lamps are updated a minimum of twice a second to protect against EMC induced corruption.

The reduced number of interface lines reduces the cost of EMC protection. The door board may have 16 outputs and 16 inputs, which would require EMC protection for 32 lines using a parallel interface. The SPI design reduces this to 5 lines requiring protection, which in this design is via opto-isolators.

The control logic and shift registers can handle only 1 SPI channel, but their data I/O to the SPI is multiplexed.

The use of up to 7 channels allows the use of smaller SPI loops that can be scanned at different rates. In particular, the door push buttons need to be scanned at a high rate, but lamps and mechanical meters are scanned at a relatively low rate.

Also, a fault in one SPI channel will not shut the other channels down. If only one channel were used for the entire machine. the scan rate would be the same for all channels and it would be more susceptible to faults.

In the slot machine. channels are:-

1. Top box lamps
2. Mechanical meters
3. Future expansion
4. Door inputs
5. Door outputs
6. Main board inputs
7. Main board security

Channel 0 is a null channel used to deselect all other channels.

Because each SPI channel is always a loop, software can detect the length of the loop to check hardware configuration and detect any hardware failures.

The advantages of driving the peripherals serially are:

- Increased expandability, more devices can be added with no additional decoding hardware
- Reduction in looming at system level
- Reduction in area at board level due to less interconnections
- No decoding hardware needed, the address of a device is fixed by the way it connects to the others in the chain
- Cost of EMC protection reduced.

The Serial Peripheral Interface channels are used in the present machine to drive:

- Slow Direct Outputs
- Alphanumeric Display
- Dot Matrix Displays
- Seven Segments LED Displays
- The Slow Inputs

The timing, shown in Figure 3 has been designed to accommodate several types of shift register devices.

The descriptions of the signals shown in Figure 3 are as follows:-

INT: The rising edge of INT generates a CPU interrupt

WRSPI: The rising edge writes 8 bit data to the shift register and triggers the control logic to start a transfer

ENABLE: Is latched from WRSPI

RENABLE: Is registered ENABLE, i.e. synchronised to the clock

Data is shifted in and out of the 8 bit data shift register on the rising edge of CLK299. SCLK is a version of CLK299 transmitted to the SPI devices. CLK299 has an extra pulse, used to write data into the 8 bit shift register.

The block diagram of the parallel/serial conversion system is given in Figure 1. Every time the processor writes a byte to the interface it is actually writing a byte into a parallel to serial converting shift register 101 and the following process is triggered:

1. The write signal is latched asserting ENABLE;
2. ENABLE is synchronised to the clock as RENABLE;
3. ENABLE generates a pulse to write the byte of data into the shift register;
4. RENABLE triggers 8 more pulses on the clock CLK 299 to shift serial data into and out of the shift register chip;
5. After the last pulse, the interrupt line is asserted, the rising edge causing an interrupt to the CPU;
6. The CPU then write the next byte, or terminates the cycle by negating NSIOE.

The output (DOUT) of the shift register 101 is distributed to one of seven SPI output channels via an SPI output bus and optocoupler 102, with the exception of one channel which is connected to the 8 bit logic door input circuit 104 on the main board and therefore does not require isolation. A one line to 8 line multiplexer 105 generates channel selection signals NSIOEO-7 which select input/output devices when they are to be connected to the SPI output bus.

Of the seven SPI input channels all except for the logic door inputs 104 and the main board inputs 107 are isolated from the main board via optocouplers 103 and all are multiplexed into the shift register 101 input (DIN) via an 8 line to 1 line multiplexer 106. Optical isolation for NSIOEO-5, which travel off of the main board, is provided by optical couplers 108. SPI channel addresses to the multiplexers 105, 106 are held in a latch 109 which is written to from the processor via the data bus BD(0.7).

Every time a byte goes out of the shift register 101 another byte goes in. The system reads the inputs by writing the outputs in a cyclic process.

The values written in certain conditions can be read back in the next scan period to check for consistency. The interface also allows the reading of status information back from devices with that facility.

All SPI signals carried off of the main board are optically coupled 102, 103, 108 (using a current loop) for inter-board isolation.

The SPI bus supports the following devices:

FUNCTION	DEVICE	DESCRIPTION
Input	74HC165	8 bit parallel in serial out shift reg.
Output	74HC4094	8 Stage Shift and Store Bus register
Output	TPIC2802	Octal intelligent power switch with serial input
Output	74HC594	8 bit Shift Reg. with output register

The following functional systems within the machine are connected via one or other SPI buses:

- Alphanumeric Display
- Mechanical meters
- Lamps
- Push button lamps (switch inputs and lamp outputs)
- Jackpot switch
- Operator switch
- Handle lock and position switches
- Bell
- Door push buttons.

A MAX 7219 LED driver chip serial interface is connected to the end of SPI loops to derive a 7 segment display. Dot matrix displays can be interfaced in the same way.

Seven segment led displays are also driven serially through SPI Channel #5. They may or may not be multiplexed (as previously described depending upon the requirements of the particular machine.

Mechanical credit meters are driven using a TPIC2802. This device can be used in two ways:

1. Located with the main logic of the machine and serially driven from the SPI bus as illustrated in Figure 4; or

2. Located on the mechanical meters board, serially driven from the SPI bus as illustrated in Figure 5.

The more attractive option is the second one. It will give the maximum flexibility and is the only way of minimising the looms. It will not require a specific line to sense disconnection of the meter, since if one meter, or the whole board, is disconnected the status read back by the processor will change sense.

The system supports up to 12 meters.

All the lamps in the present machine, with the exception of the Stepper Reel Indicators lamps, are driven using a TPIC2802 from Texas Instruments.

The present machine also supports a light tower which is connected to a connector on either the top box distribution or mechanical meter board, both of which use TPIC2802 and SPI interface. The connector is called "Top Box Connector". Four light-tower lamps are supported.

The top box also provides animation lamps which are driven using TPIC2802 serial drivers and the first SPI bus.

The system will drive 24 lamps. If more lamps are required the serial nature of the SPI bus allows for a second Distribution Board to give extra lamps.

Both solutions can be combined in machines with mechanical meters to give more lamps.

The door buttons contain both lamps and switches.

A maximum of 16 buttons and 32 lamps are supported. The buttons are read through a shift register and the lamps driven through a TPIC2802.

Each button and the lamp that it contains are handled from the same connector on the Distribution Board mounted in the door. There are 16 connectors on each distribution board to handle 16 lamps and buttons.

The Jackpot switch is a Slow Direct Input and is connected along with the Operator Switch (also a Slow Direct Input) via a single connector.

These inputs are Schmitt trigger inputs with pull up resistors. The switches connect the inputs to ground. The ground lines use an RC filter for ESD and EMI suppression and rejection.

Those machines fitted with a handle have two microswitches to give the position of the handle, and a solenoid to lock the handle so that it cannot be pulled unless enabled by software control.

The SPI bus is implemented on an SPI bus driver and interface board. The bus is multiplexed into 7 separate channels, of which only one channel is accessible at any given time.

Channel

#	Name	Type	Description	Comment
1	SNPIxCLR	OUTPUT	SPI Channel x Clock	Bit clock. This can be common for all the channels
2	NSPIxSTB	OUTPUT	SPI Channel x Strobe	Enable line for the channel. There ,must be one independent line per channel
3	NSPIxCLR	OUTPUT	SPI Channel x Clear	Reset line to the channel. It can be common for all the channels except mechanical meters (2) and logic door security (7)
4	SPIxDIN	INPUT	SPI Channel x Data Input	There must be one independent line per channel
5	SPIxDOU	OUTPUT	SPI Channel x Data Output	There can be one common line for all the channels

The SPI signals have the following specifications:

-Optically coupled (inputs and outputs)

-Connected via a low pass filter of 80 KHz +/- 15% bandwidth, using ceramic capacitors

-The inputs are connected via Schmitt Triggers

-The outputs are NPN open collector type

-The outputs are protected against a 1 sec short circuit to +23 Volts

The baud rate (bit clock) of the SPI is 8 KHz and the inputs and outputs are referenced to the +22 Volts/+9 Volt ground.

As illustrated in Figure 6, the SPI driver board supports 7 SPI channels selected via 3 bits in an output register.

On reset of the SPI bus the following conditions should apply:

- The channel #0 is automatically selected
- The reset line to the channels is active
- The clock line is not active
- The SPI interrupt is disabled

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

CLAIMS:

1. A peripheral interface system for a digital processor. the interface including parallel input/output (I/O) means arranged to interface with a parallel input/output bus of a digital processing unit, parallel to serial conversion means arranged to convert a data word from the parallel I/O bus to a serial data string on a serial output data line of a serial bus. serial to parallel conversion means arranged to convert a serial data string on a serial input data line of the serial bus to a data word on the parallel I/O bus. clock means arranged to provide timing signals for the interface and control means arranged to control the transfer of data between the parallel I/O bus and the peripheral serial bus, the control means also providing a bus clock, a data enable signal, and a reset signal on the serial bus in addition to the input and output serial data lines.

2. The peripheral interface system of claim 1 wherein a plurality of serial buses are provided, each connected in parallel to the serial to parallel and parallel to serial conversion means, the clock means and the control means, there being a separate data enable signal for each channel.

3. The peripheral interface system of claim 2 wherein 7 serial channels are provided for each parallel interface.

4. The peripheral interface system of claim 1, 2 or 3 wherein a distribution board is provided to interconnect with the serial bus to demultiplex the serial bus output signals and to drive output devices and/or to receive input signals from input devices and to multiplex these into serial bus signals.

5. A slot machine including game playing means and control means wherein the game playing means includes at least one peripheral device and the control means includes a digital processor, and communication between the control means and the at least one peripheral device is via a serial interface system including parallel input/output (I/O) means arranged to interface with a parallel input/output bus of a digital processing unit. parallel to serial conversion means arranged to convert a data word from the parallel I/O bus to a serial data string on a serial output data line of a serial bus, serial to parallel conversion means arranged to convert a serial data string on a serial input data line of the serial bus to a data word on the parallel I/O bus, clock means arranged to provide timing signals for the interface and control means arranged to control the transfer of data between

the parallel I/O bus and the peripheral serial bus, the control means also providing a bus clock, a data enable signal, and a reset signal on the serial bus in addition to the input and output serial data lines.

6. The slot machine of claim 5 wherein a plurality of serial buses are provided, each connected in parallel to the serial to parallel and parallel to serial conversion means, the clock means and the control means, there being a separate data enable signal for each channel.

7. The slot machine of claim 6 wherein 7 serial channels are provided for each parallel interface.

8. The slot machine of claim 5, 6 or 7 wherein a distribution board is provided to interconnect with the serial bus to demultiplex the serial bus output signals and to drive output devices and/or to receive input signals from input devices and to multiplex these into serial bus signals.

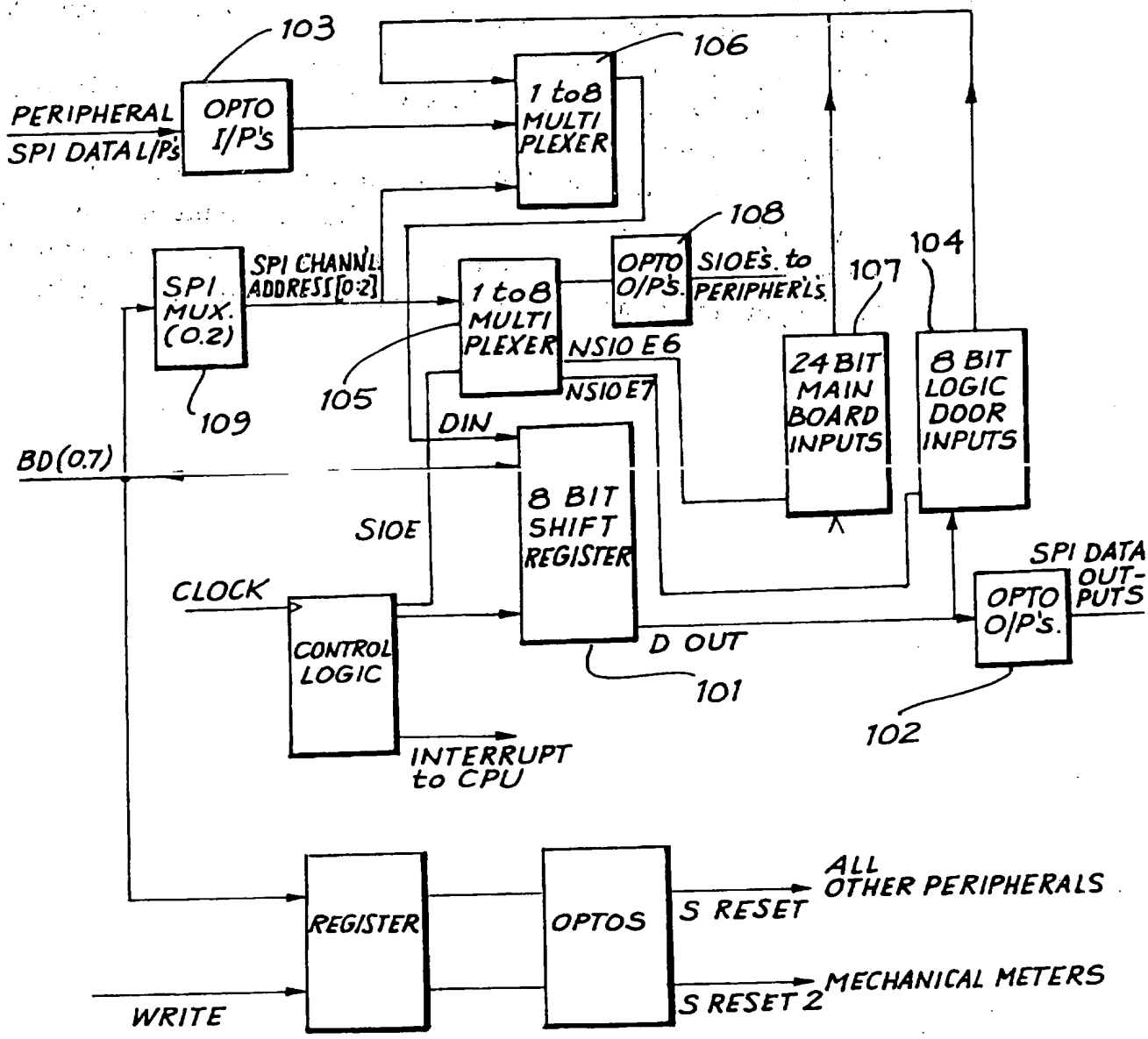
103
106
PERIPHERAL SPI DATA I/P's
OPTO I/P's
1 to 8 MULTI PLEXER
108
104
SPI MUX. (0.2)
SPI CHANNEL ADDRESS [0:2]
1 to 8 MULTI PLEXER
OPTO O/P's.
SIOE's. to PERIPHERALS
107
NSIO E6
NSIO E7
105
109
DIN
24 BIT MAIN BOARD INPUTS
8 BIT LOGIC DOOR INPUTS
BD(0.7)
8 BIT SHIFT REGISTER
SIOE
SPI DATA OUT-PUTS
CLOCK
OPTO O/P's.
CONTROL LOGIC
D OUT
101
102
INTERRUPT to CPU
REGISTER
OPTOS
ALL OTHER PERIPHERALS
S RESET
MECHANICAL METERS
S RESET 2
WRITE

FIG. 1

PALASM SOURCE FILE for SPIGAL

```
PALASM DESIGN DESCRIPTION
SPI INTERFACE
------------------------------ DECLARATION SEGMENT ----------

  SHEADE :   F:\muir\pvcs\archive\spi.pdv  1.0  20 DEC 1993 17:07:16
MUIR $

TITLE    SPI.PDS
PATTERN  A
REVISION 0
AUTHOR   ROBERT MUIR
COMPANY  ARISTOCRAT
DATE     26/8/1994

CHIP     _SPI1   PALCEL 6V8
------------------------------ PIN DECLARATIONS -------------

PIN 1       clk      ; clock
PIN 2     /RESET     ; RESET
PIN 3     /WRSPI     ; WRITE cs
PIN 4      nc
PIN 5      nc
PIN 6      nc
PIN 7      nc
PIN 8      nc
PIN 9      nc
PIN 10     Gnd      ;
PIN 11     oe
PIN 12     clk299   ; COUNT BIT 0
PIN 13     /sclk    ; COUNT BIT 1
PIN 14     c2     ;
PIN 15     c3     ;
PIN 16     c4     ;
PIN 17     int      ; SPI INTERRUPT
PIN 18     ENABLE
PIN 19     RENABLE   REG
PIN 20     vcc
;------------------------------ BOOLEAN EQUATION SEGMENT ------
EQUATIONS
ENABLE    = (WRSPI + (ENABLE * /(c4 * c3 * c2 * sclk))) * /RESET
RENABLE := ENABLE
clk299    = /sclk * /WRSPI;
int       := /RENABLE;
sclk   := / RESET * RENABLE * /sclk;
c2     := / RESET * RENABLE * (c2 :+: (sclk))
c3     := / RESET * RENABLE * (c3 :+: (c2 * sclk))
c4     := / RESET * RENABLE * (c4 :+: (c3 * c2 * slk))
```

FIG. 2

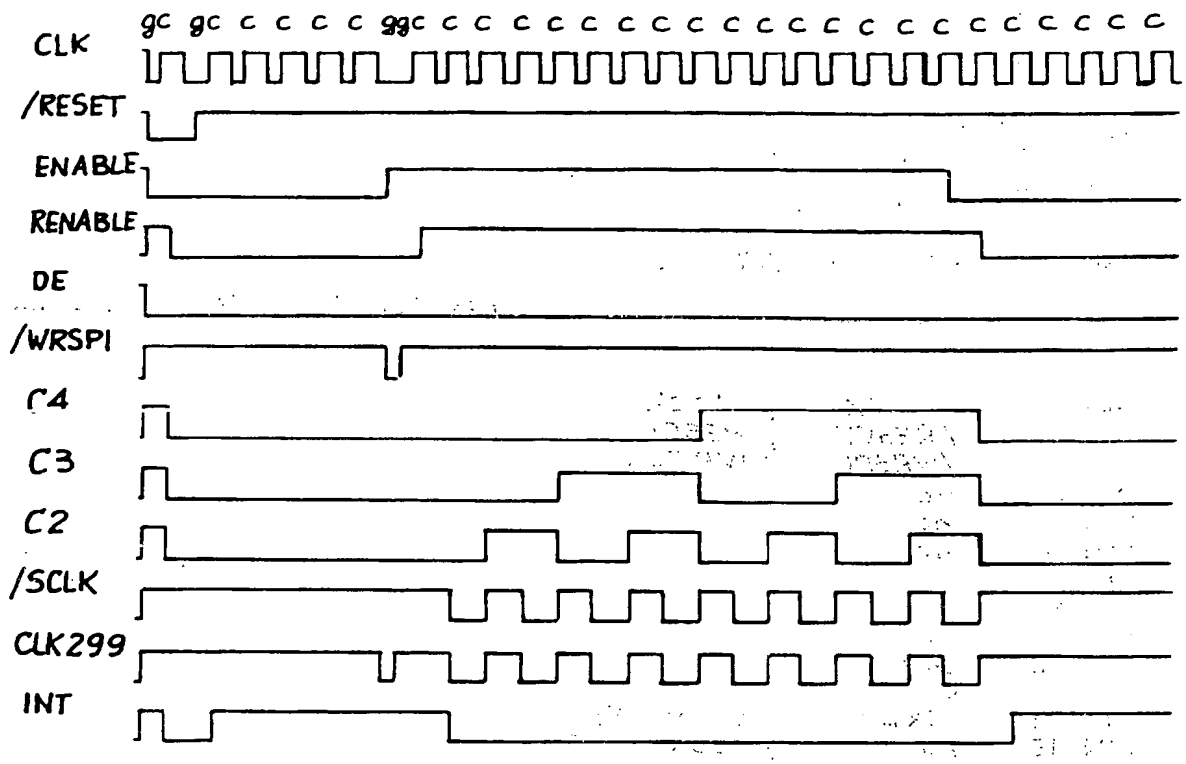

FIG. 3

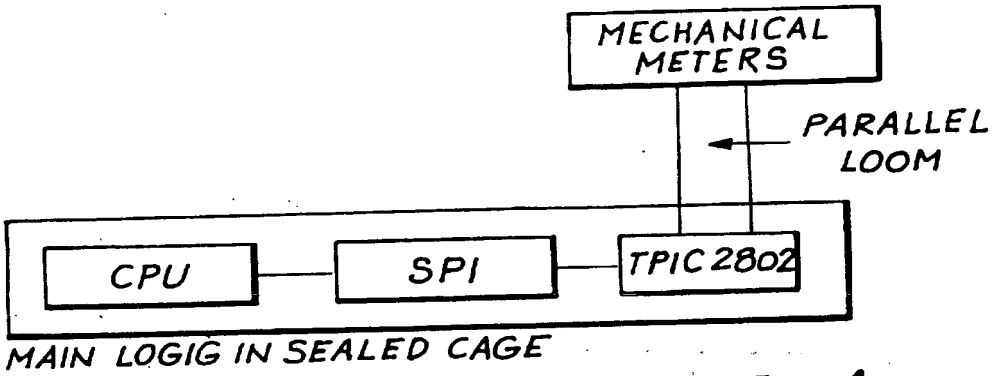
MECHANICAL METERS
PARALLEL LOOM
CPU
SPI
TPIC 2802
MAIN LOGIG IN SEALED CAGE

FIG. 4

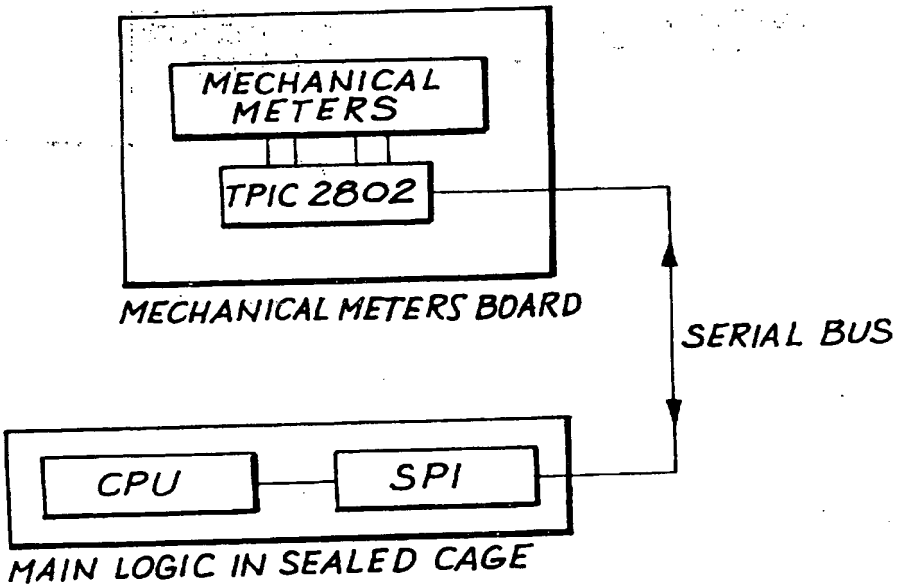
MECHANICAL METERS
TPIC 2802
MECHANICAL METERS BOARD
SERIAL BUS
CPU
SPI
MAIN LOGIC IN SEALED CAGE

FIG. 5

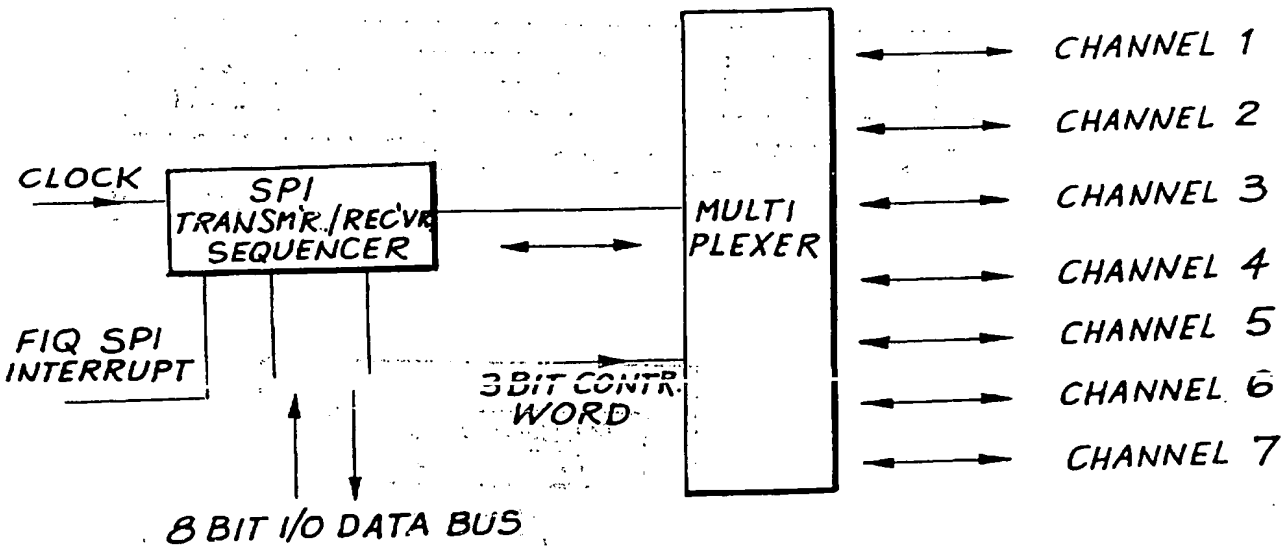
CLOCK
SPI TRANSM'R./REC'VR SEQUENCER
MULTI PLEXER
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
CHANNEL 5
CHANNEL 6
CHANNEL 7
FIQ SPI INTERRUPT
3 BIT CONTR. WORD
8 BIT I/O DATA BUS

FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00013

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: H03M 9/00, H03K 19/0175, G07F 17/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC[6] : as above

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU IPC : as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT: JAPIO: INSPEC: COMPENDEX PL: (PARALLEL: SERIAL: INTERFACE)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"The Versatile SPI" Part 1 & 2 From Electronic Engineering, Oct. 1989 pp. 61-64 and November 1989 pp. 39-44	1
Y	WO 94/10636 (The 3DO Company) 11 May 1994, whole document	1
Y	WO 93/25028 (ABB Strömberg Kojeet OY) 9 December 1993, whole document	1

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
8 March 1996

Date of mailing of the international search report
20TH MARCH 1996.

Name and mailing address of the ISA/AU
AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION
PO BOX 200
WODEN ACT 2606
AUSTRALIA Facsimile No.: (06) 285 3929

Authorized officer
John Thomson
J.W. THOMSON
Telephone No.: (06) 283 2214

Form PCT/ISA/210 (second sheet) (July 1992) cophin

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00013

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP,A2, 443420 (Bally Manufacturing) 28 August 1991, Abstract, Fig. 2	1, 5
Y	GB 2200779 (JPM Ltd) 10 August 1988, whole document	1,5
Y	GB 2139390 (Ainsworth Nominees) 7 November 1984, whole document	1, 5

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No.
PCT/AU 96/00013

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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END OF ANNEX